Fast-Tuning CMOS Microring Filters for DWDM Links with Optical Circuit Switching

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Abstract: Fast-tuning adiabatic microring channel drop filters in 45nm CMOS achieve 6.7MHz modulation bandwidth and 1.9nm O-band tuning range with sub-mW forward bias power, enabling rapidly reconfigurable DWDM receivers for datacenter networks with optical circuit switching.

Dense wavelength division multiplexing (DWDM) optical links based on microring resonator (MRR) channel drop filters allow for high-bandwidth, low-latency communications with lower power and die area than competing technologies for co-packaged optics [1, 2]. Horizontal scaling of datacenter optical networks in service of the growing demands of machine learning and artificial intelligence has led to the adoption of free-space MEMS micromirror array based optical circuit switches (OCSes) [3] to create dynamically-reconfigurable optical interconnects. Their high cost and ∼10 ms switching time have, however, limited the adoption of such OCSes to higher layers of the network. OCSes capable of µs reconfiguration are needed to lower response time to bursts in network traffic as well as to enable high performance application-specific network schedules [3]. With next-generation silicon photonics MEMS-based OCSes achieving sub-µs switching times [4], the latency becomes dominated by the microring-based DWDM receiver bank's re-acquisition and locking time to the new transmitter bank's laser wavelengths, since there will be variation between lasers at different parts of the network if they are cost and power optimized [5]. Conventional wavelength acquisition via thermal tuning is limited to ms timescales by slow thermal time constants on the order of tens of µs [6]. To address this bottleneck, we present fast-tuning and efficient microring drop filters based on forward-bias carrier injection parallel to the optical mode propagation direction.

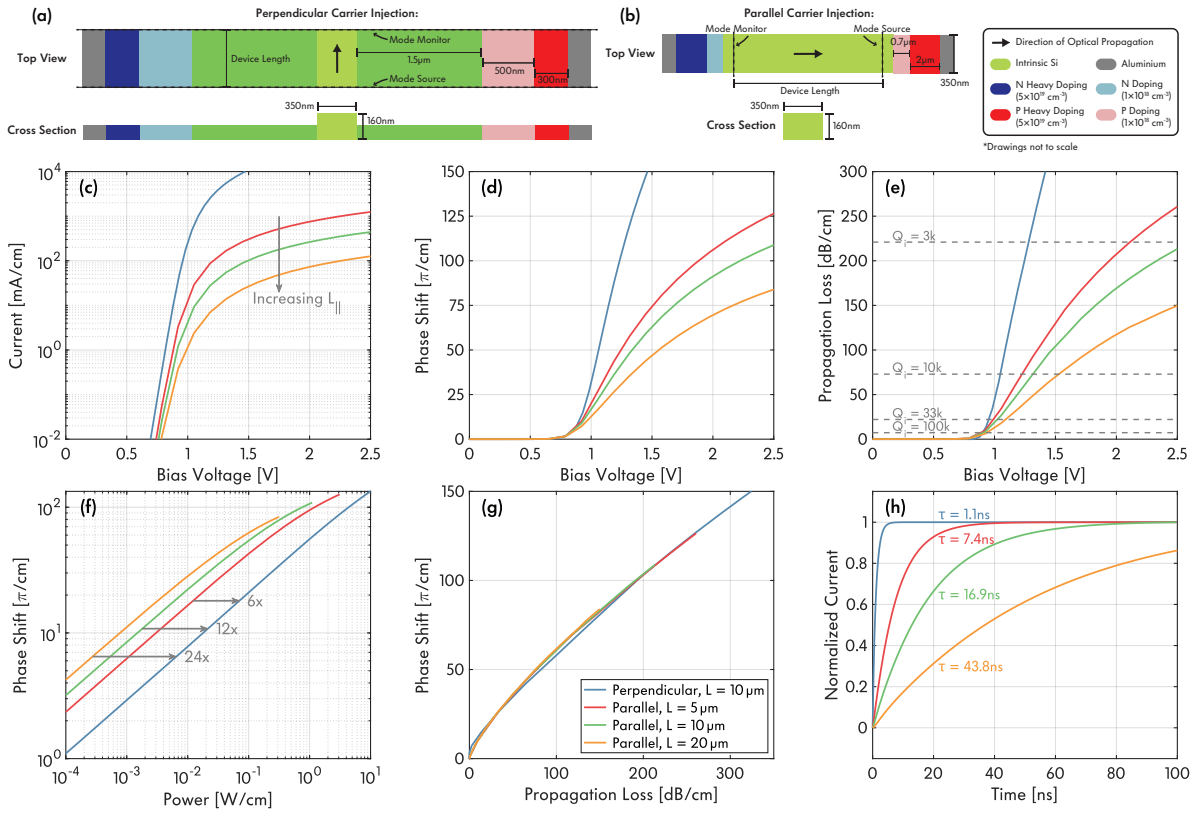

Fig. 1: Simulation setups for (a) conventional perpendicular carrier injection and mode propagation in a rib waveguide and (b) proposed parallel carrier injection and mode propagation in a slab waveguide. Simulation results normalized to 1cm total length for (c) IV curves using Lumerical CHARGE (a typical Si-SiO_2 surface recombination velocity of 100 cm/s would result in <10% reduction in current), (d) optical phase shift vs forward-bias voltage, (e) optical loss vs forward-bias voltage with microring intrinsic Q-factors marked assuming a typical value of $n_{group} = 3.5$, (f) optical phase shift vs static power showing the benefit of parallel carrier injection, (g) phase shift vs loss showing the same fundamental curve for all configurations, and (h) electrical step responses showing slower modulation speed for higher-efficiency phase shifters due to the longer transit time. Lumerical FDTD is used for all optical simulations with imported carrier densities from Lumerical CHARGE.

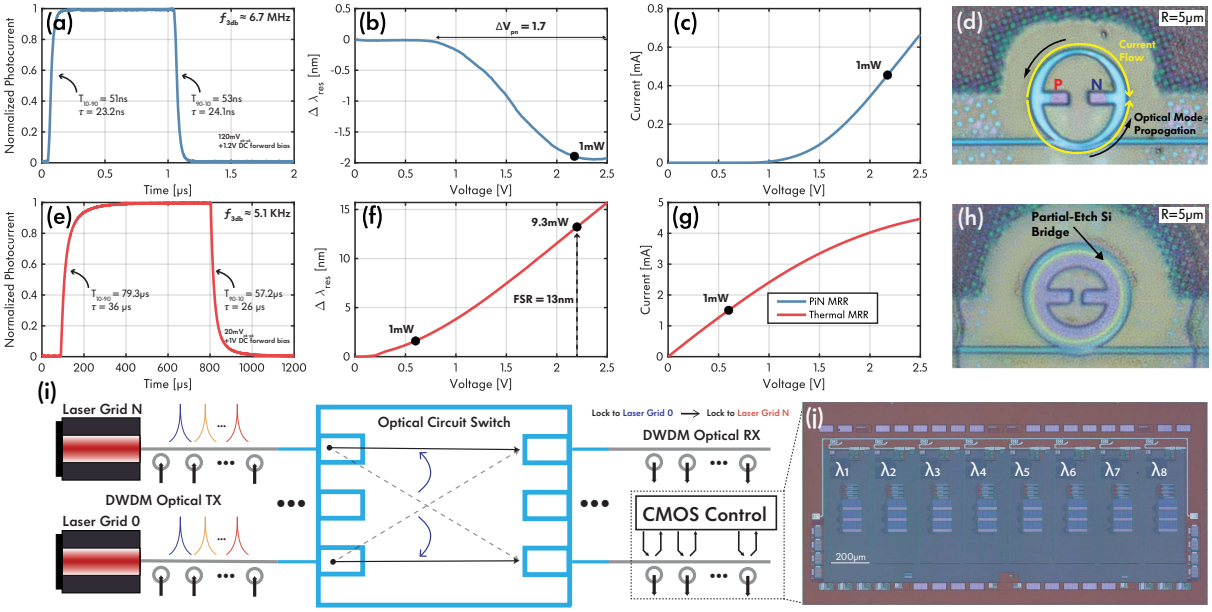

Fig. 2: (a,e) Electro-optical step responses, (b,f) resonance shift efficiencies, (c,g) IV curves, and (d,h) micrographs of 5µm-radius adiabatic *p-i-n* carrier injection MRR and 5µm-radius thermally-tuned MRR on the same die. (i) Conceptual schematic of an OCS network fabric switching a DWDM receiver between two transmitter banks with mismatched laser grids. (j) Micrograph of a DWDM receiver bank based on adiabatic *p-i-n* MRR channel drop filters with integrated CMOS control circuits in GlobalFoundries' 45SPCLO CMOS photonics process.

Fig. 1 presents a TCAD and FDTD simulation study showing that parallel carrier injection structures directly trade modulation speed for energy efficiency, while maintaining low drive voltage requirements and following the same fundamental loss versus phase shift tradeoff curve as all free carrier plasma dispersion electro-optic modulators. Rather than inject and then quickly extract charge carriers along the entire length of the waveguide in perpendicular to the direction that light propagates, alternating *p*- and *n*-doped contacts can be placed periodically along the length of the waveguide to inject carriers in parallel with the propagation of the optical mode, which is approximated by the linear slab waveguide simulation setup in Fig. 1. They are then extracted after a much longer transit time, effectively being "reused" over a larger volume of the waveguide during their lifetime to create more phase shift for the same current level. The highly nonlinear exponential IV curves of *p-i-n* diodes make the required voltage swing scale-up more slowly than the net phase shift, reducing the power consumption for producing a given shift as the parallel injection contacts are moved further apart (i.e. doubling the intrinsic width is *not* the same as putting two *p-i-n* diodes in series). Forward-bias modulators are already known for having high shift per volt, but improved energy efficiency reduces self-heating that normally limits their overall tuning range.

Applying this concept to a fast-tunable channel drop filter, we improved our previous adiabatic microring design optimized for carrier extraction in reverse bias with graded dopings [7] with wider, heavily-doped contacts to reduce access resistance and increase the forward-bias IV curve slope, and ported the design to O-band with increased FSR (reduced radius) for datacom applications. For a fair comparison, we also designed a highly-optimized thermally-tuned microring with an undercut silicon heater bridged by partial etch silicon to the waveguide to maximize its efficiency. Fig. 2 presents measurements of the key performance metrics of both devices, which are fabricated in Globalfoundries' 45SPCLO CMOS photonics process to enable monolithic integration with high-speed CMOS microelectronics. We achieve greater wavelength tuning range than thermal tuning at similar static power consumption (1mW), and with $>1000\times$ faster modulation bandwidth and intrinsic Q-factors [8] still suitable for DWDM channel optical bandwidths. Fig. 2(j) shows a micrograph of an 8-channel DWDM receiver bank based on this device, integrating high-speed receivers, control logic, and 1.8V-swing CMOS DACs with fast-tuning *p-i-n* MRRs on the same die to quickly acquire and lock to a DWDM grid.

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